ADwin

Hardware Manual

Version 1.3

August 1998

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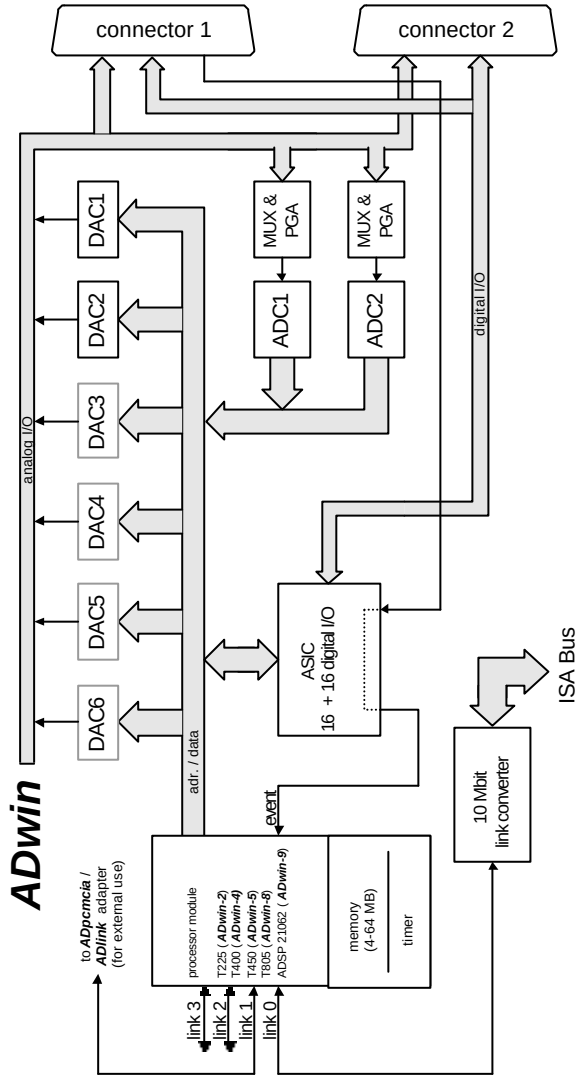

Figure 1: Block diagram of the ADwin board with changeable processor module

1 A brief Overview

The ***ADwin-light*** board has a plug-in device for an 8/16-bit ISA-slot (Industry Standard Architecture) in an IBM-compatible PC. It needs a long slot.
The board includes its own processor for data acquisition and control and can be divided into two parts: the data acquisition board and the plug-in processor module.
As shown in the block diagram (Figure 1) the two ADCs, the DACs and the digital input/output registers can be directly accessed by memory addresses. Each CPU has one or more links for fast data transfer. Link #0 of each processor module is connected to the PC by a linkadapter component, which adapts the serial link connection to the 8-bit wide PC I/O bus. This link connection is also used for downloading the transputer program to the board memory.
The board has 2 ADCs with 12-bit resolution and a conversion time of 8.5 microseconds; they can be operated, according to the application, simultaneously or asynchronously. Before each ADC there is a programmable amplifier (gains 1, 2, 4 or 8) and a multiplexer with 8 inputs.
As standard version 2 DACs with 12-bit resolution are included on the board. When needed, the board can be equipped with up to 6 DACs.
The DACs have a second buffer for latching so that with an instruction new data can be output on all DACs at the same time. In addition the board contains 16 digital inputs and outputs as well as a trigger input.

2 Installation of the *ADwin* board

Please, pay attention to the following notes before installing the ***ADwin*** board:

- Touch the ***ADwin*** board only at the upper edge in order to avoid damage of the board components.
- The base address for the linkadapter on the ***ADwin*** board has the default address 150h. If you wish to set a different address, refer to chapter 3.3 (Setting the I/O-address).
- The input and output voltage ranges of the ADCs and DACs, respectively, have the default setting of ±0 V. If you wish to set a different voltage range, refer to chapter 3.1 (Setting the input voltage range of the ADC) 3.2 (Setting the output voltage range of the DACs) respectively.

In order to install the ***ADwin*** board, follow the instructions below:

1. Make sure that the power switch on your PC is turned "off".
2. Open the computer chassis according to your PC manual.
3. Choose an empty plug-in slot and make sure that there will be enough space for installation of the ***ADwin*** board.
4. Remove the board access cover at the rear of the PC which belongs to the slot you have chosen to install the board.
5. Plug-in the ***ADwin*** board carefully into the slot chosen.
6. Secure the board access cover at the rear of the PC with the screws removed (under point 4).
7. Replace the computer chassis.

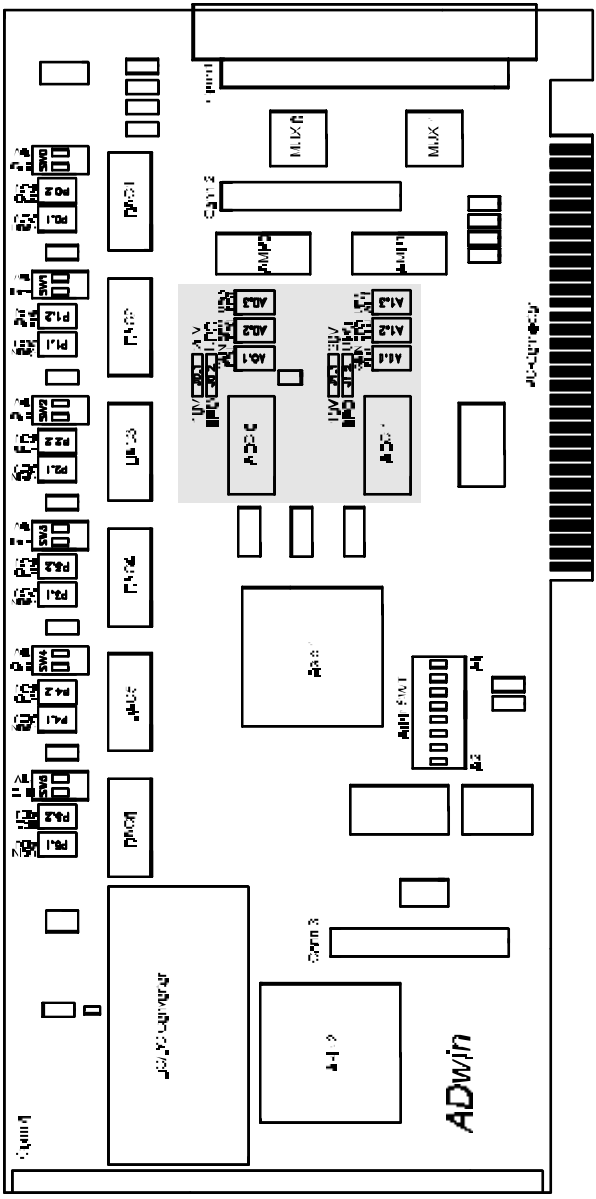

Figure 2: Position of jumpers and potentiometers for setting the ADCs

3 Jumper settings

3.1 Setting the input voltage range of the ADC

Each ***ADwin*** board has two ADCs whose input voltage range can be adjusted by the jumpers Jx.1 and Jx.2 (s. Figure 2). The „x“ in the potentiometer title stands for the number of the corresponding ADC. The following settings are possible:

Jx.1	Jx.2	voltage range
BPO	10V	±V
BPO	20V	±0V (default setting)
UPO	10V	0...10V
UPO	20V	**not allowed**

For calibration of offset and gain there are three potentiometers.

Note: These potentiometers were optimally adjusted after the final test of the board. Therefore we kindly ask you not to change the settings of the potentiometers unnecessarily, because this will lead to inaccuracy.

potentiometer	calibration of
Ax.1	gain factor
Ax.2	offset (bipolar mode)
Ax.3	offset (unipolar mode)

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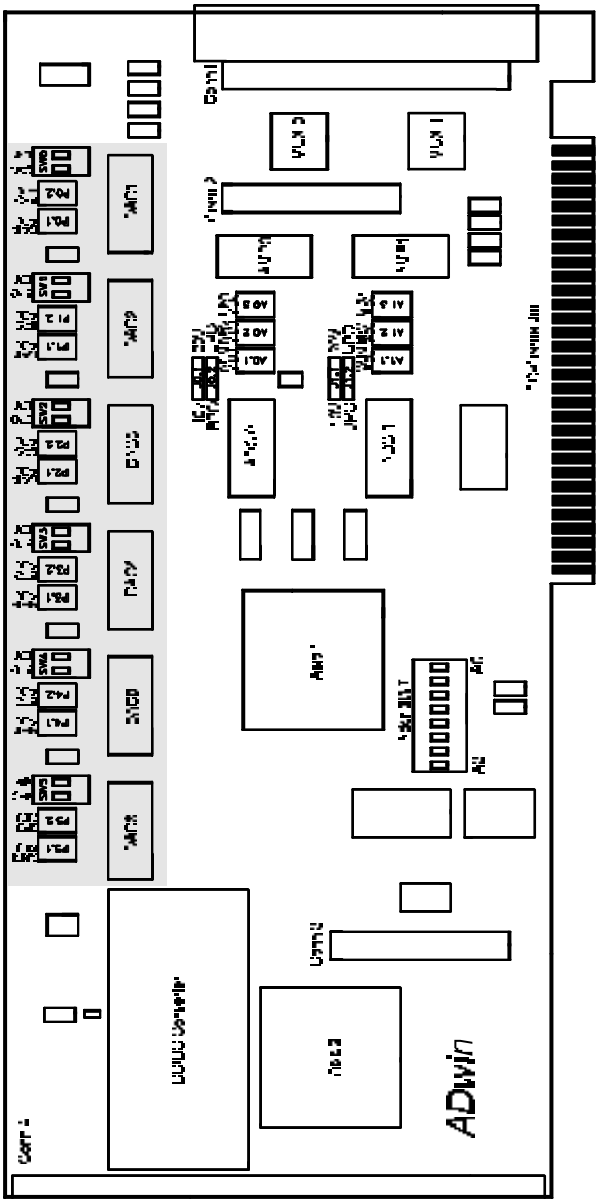


Figure 3: Position of jumpers and potentiometers for setting the DACs

3.2 Setting the output voltage range of the DACs

Each ***ADwin*** board has at least two DACs whose output voltage range can be adjusted by the jumpers located just above the DACs (s. Figure 3).
The following settings are possible:

switch 1	switch 2	voltage range
BPO	10V	±5V
BPO	20V	±10V (default setting)
UPO	10V	0...10V
UPO	20V	**not allowed**

Example: Jumper position for the input voltage range 0...10 V

For calibration of offset and gain there are two potentiometers for each DAC. The „x“ in the potentiometer title stands for the number of the corresponding ADC.

Note: These potentiometers were optimally adjusted after the final test of the board. For that reason we kindly ask you not to change the settings of the potentiometers unnecessarily, because this will lead to inaccuracy.

potentiometer	calibration of
Px.1	gain factor
Px.2	offset

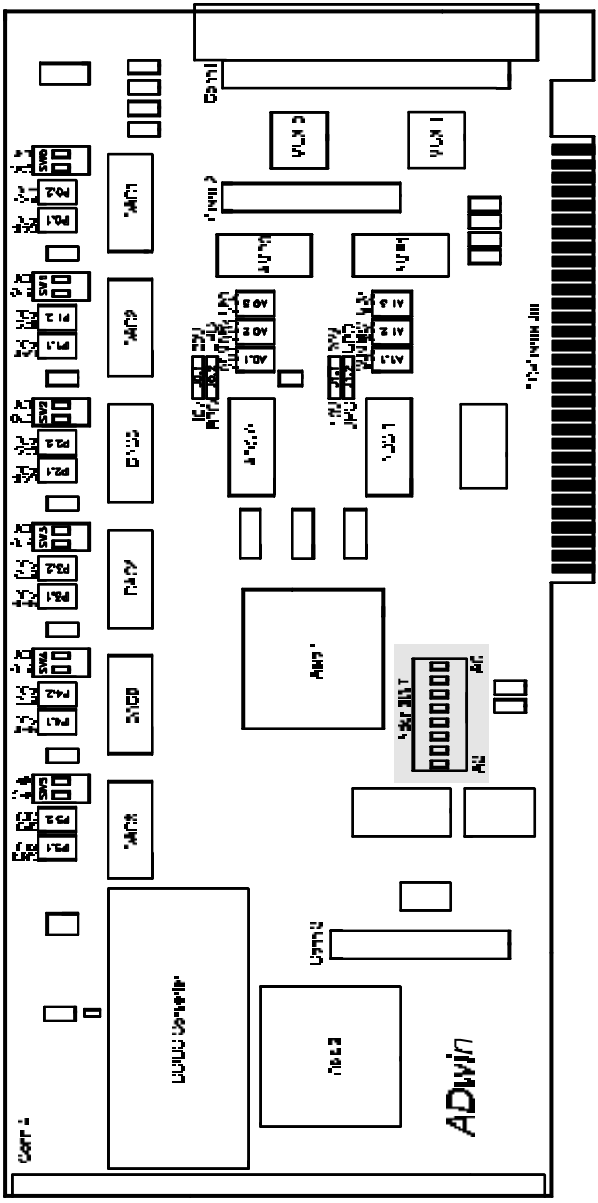


Figure 4: Jumper position for setting the I/O base address

3.3 Setting the I/O-address

Setting the I/O-address (base address for the linkadapter of the ***ADwin*** board) is made by the DIP-switch called ADDR SWITCH (s. Figure 4).
The base address can be set on the DIP-switch in binary code beginning with the third address bit.

Example: The default setting 150h of the base address in ***ADbasic*** and on the ***ADwin*** board is in binary code 01 0101 0000. The two least significant bits are to be omitted (01 0101 00~~00~~). All numbers "1" are to be set in reverse order to "ON" on the DIP-switch:

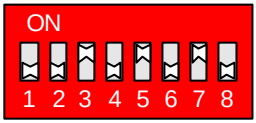


Figure 5: DIP-switch with the base address 150h

base address	**switch no.**							
	1	**2**	**3**	**4**	**5**	**6**	**7**	**8**
150h	OFF	OFF	ON	OFF	ON	OFF	ON	OFF
190h	OFF	OFF	ON	OFF	OFF	ON	ON	OFF
200h	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
300h	OFF	OFF	OFF	OFF	OFF	OFF	ON	ON

Note: In case of using a different base address than 150h, this address has to be indicated in ***ADbasic*** and in the TestPoint objects.

3.4 Calculation of the ADC/DAC values

The ADC as well as the DACs used for the ***ADwin*** board have a resolution of 12 bits and divide the chosen measurement range into 4096 steps.

Gain = 1:

Adjust: 0...10 Volts:
An ADC value of 0 corresponds to the voltage of 0 Volts
An ADC value of 4096 corresponds to the voltage of 10 Volts
An ADC digit corresponds to 10 Volts/4096 = 2.44 mV

Adjust: ±5 Volts:
An ADC value of 0 corresponds to the voltage of -5 Volts
An ADC value of 2048 corresponds to the voltage of 0 volts
An ADC value of 4096 corresponds to the voltage of +5 Volts
An ADC digit corresponds to 10 Volts/4096 = 2.44 mV

Adjust: ±10 Volts:
An ADC value of 0 corresponds to the voltage of -10 Volts
An ADC value of 2048 corresponds to the voltage of 0 Volts
An ADC value of 4096 corresponds to the voltage of +10 Volts
An ADC digit corresponds to 20 V/4096 = 4.88 mV

Gain > 1:

If the gain factors of the additional gains are selected higher than 1, the calculated voltage has still to be divided by the selected gain.

The voltage can be calculated according to the following formula:

$$Voltage = (Digits - 2048_{bipolarity}) * \frac{Voltage\,\text{range}}{4096 * gain}$$

In case of using the unipolar setting, the offset of 2048 digits has to be ignored.

4 Pin assignment

4.1 The I/O-socket at the rear of the board

At the rear of the board there is a 37-pin D-sub socket. The socket has

- 4 analog outputs,
- 6 analog inputs,
- 6 digital inputs,
- 6 digital outputs,
- 1 trigger input and
- the power supply of the PC (unfused)

connected to it (s. Figure 6).

On demand you can attach filter modules or isolation amplifiers to the connector.

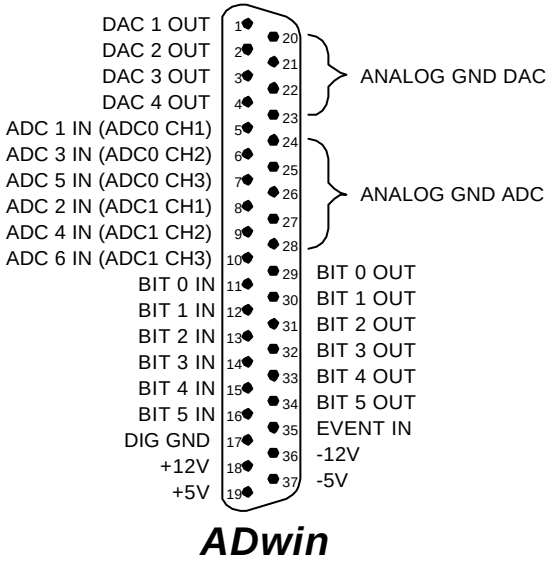
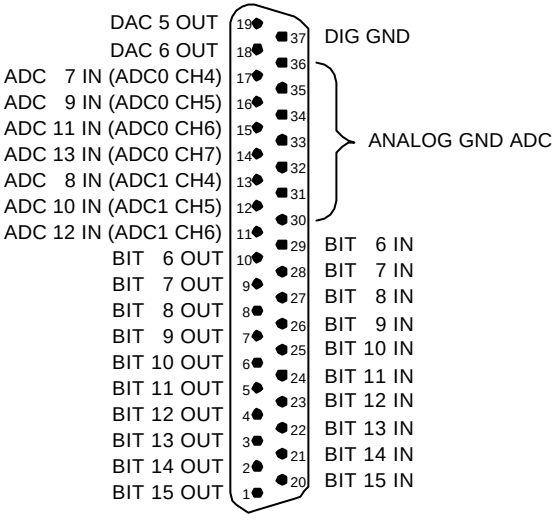


Figure 6: Pin assignment of the 37-pin D-sub connector

4.2 I/O-add-on connector

4.2.1 Add-on connector for 12 analog inputs and 32 digital I/Os

Additional inputs and outputs which cannot be added to the I/O-socket, are placed on the connectors **Conn2** and **Conn3**. These connectors can be connected by the supplied grey add-on cable with a D-sub connector on a second plate (called: ***12-AIn***). The pin assignment of the D-sub add-on connector is shown in figure 7a.

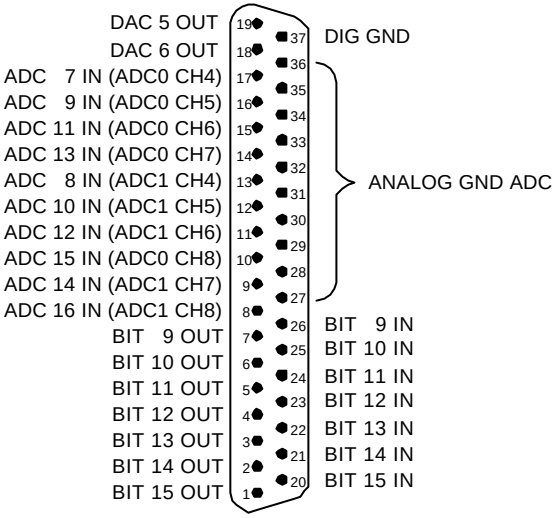


ADwinadd-on connector (13 AIN / 32 DIO)

Figure 7a: Pin assignment of the 37-pin D-sub add-on connector (male) for 13 AINs and 32 DIOs

4.2.2 Add-on connector for 16 analog inputs and 26 digital I/Os

Additional inputs and outputs which cannot be added to the I/O-socket, are placed on the connectors **Conn2** and **Conn3**. These connectors can be connected by the supplied multicolor add-on cable with a D-sub connector on a second plate (called: ***16-AIn***). The pin assignment of the D-sub add-on connector is shown in figure 7b.



ADwinadd-on connector (16 AIN / 26 DIO)

Figure 7b: Pin assignment of the 37-pin D-sub add-on connector (male) for 16 AINs and 26 DIOs

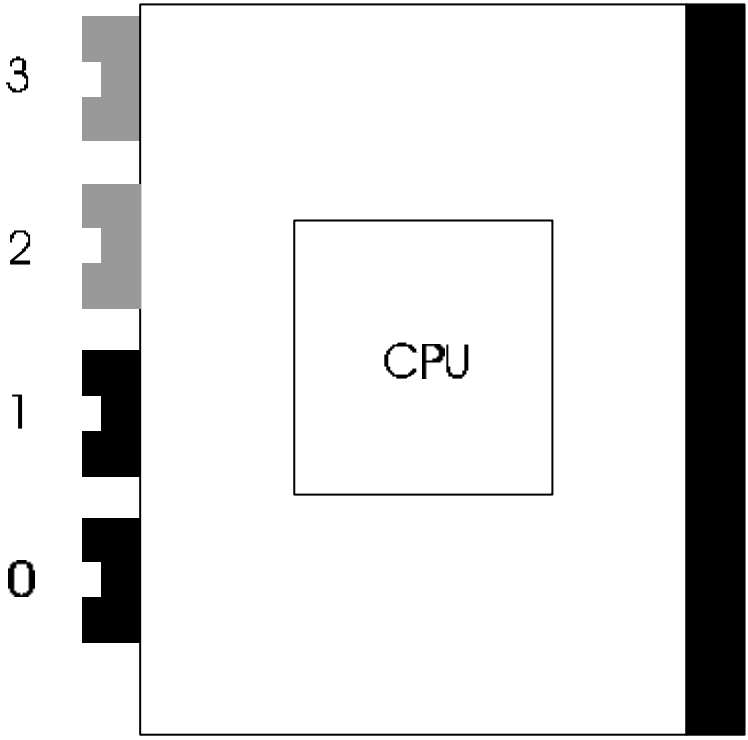


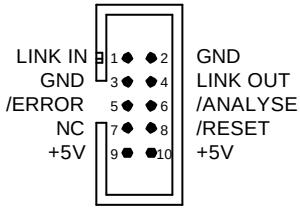
Figure 8: Position of the link connectors

4.3 The link connectors of the processor module

The link connectors of the CPU are connected with the connectors at the front of the processor module. The assignment of the connectors to the links can be seen in Figure 8. The pin assignment of the link connector is shown in Figure 9.
The ***ADwin-2*** (T225), ***ADwin-5*** (T450) and ***ADwin-8*** (T805) have four links. The ***ADwin-4*** board (T400) has two and the ***ADwin-9*** (ADSP 21062) has one link.

Note: Link #2 at the ***ADwin-9*** board is only used for stability when the board is installed in an ***ADwin-Pro*** system. No data transfer is possible with this link.

The link speed is set to 10 MBit/s. For installation in the PC, Link 0 of the processor module is fixed to the linkadapter of the measurement data acquisition board and is used for data exchange with the PC.
The remaining links can be used to link the ***ADwin*** board to other processor modules. For standard operations of the ***ADwin*** board these linkadapters are not necessary.



link-connector (CPU)

Figure 9: Pin assignment of the link connector

5 The I/O-addresses on the CPUs

5.1 ADwin-2 (T225)

In order to get very short access times, the data and control registers of the ADCs and DACs are located directly in the memory address area of the CPU.

Address	Bit no.	Function	
7F00h		control of multiplexers & programmable amplifiers	
	0-2	multiplexer ADC1	
	3-5	multiplexer ADC2	
	6, 7	amplifier for ADC1	
	8, 9	amplifier for ADC2	
7F08h		start conversion of ADCs & DACs output.	Write 0 in corresponding bit to start conversion. All three functions can be initiated with a single instruction simultaneously.
	0	start_Conv. ADC1	
	1	start_Conv. ADC2	
	2	start_out all DACs	
7F10h		status bit of ADCs.	During conversion bits are set to 1.
	0	end_of_conv ADC1	
	1	end_of_conv ADC2	
7F18h	0-11	data register ADC1	After end-of-conversion, result in last 12 bits.
7F20h	0-11	data register ADC2	
7F28h	0-11	data register DAC1	Values to converted should be written into last 12 bits. To start conversion set bit 2 at address 7F08h to 0.
7F30h	0-11	data register DAC2	
7F38h	0-11	data register DAC3	
7F40h	0-11	data register DAC4	
7F48h	0-11	data register DAC5	
7F50h	0-11	data register DAC6	
7F58h	0-15	digital input register	
7F60h	0-15	digital output register	

5.2 ADwin-4, ADwin-5 and ADwin-8 (T400, T450 and T805)

In order to get very short access times, the data and control registers of the ADCs and DACs are located directly in the memory address area of the CPU.

Address	Bit no.	Function	
00h		control of multiplexers & programmable amplifiers	
	0-2	multiplexer ADC1	
	3-5	multiplexer ADC2	
	6, 7	amplifier for ADC1	
	8, 9	amplifier for ADC2	
10h		start conversion of the ADCs & DACs output	Write 0 in corresponding bit to start conversion. All three functions can be initiated with a single instruction simultaneously.
	0	start_Conv. ADC1	
	1	start_Conv. ADC2	
	2	start_out all DACs	
20h		status bit of ADCs.	During conversion bits are set to 1.
	0	end_of_conv ADC1	
	1	end_of_conv ADC2	
30h	0-11	data register ADC1	After end-of-conversion, result in last 12 bits.
40h	0-11	data register ADC2	
50h	0-11	data register DAC1	Values to converted should be written into last 12 bits. To start conversion set bit 2 at address 10h to 0.
60h	0-11	data register DAC2	
70h	0-11	data register DAC3	
80h	0-11	data register DAC4	
90h	0-11	data register DAC5	
A0h	0-11	data register DAC6	
B0h	0-15	digital input register	
C0h	0-15	digital output register	

5.3 ADwin-9 (ADSP 21062)

In order to get very short access times, the data and control registers of the ADCs and DACs are located directly in the memory address area of the CPU.

Address	Bit no.	Function	
20400000h		control of the multiplexers & programmable amplifiers	
	0-2	multiplexer ADC1	
	3-5	multiplexer ADC2	
	6, 7	amplifier for ADC1	
	8, 9	amplifier for ADC2	
20400010h		start conversion of the ADCs & DACs output.	Write 0 in corresponding bit to start conversion. All three functions can be initiated with a single instruction simultaneously.
	0	start_Conv. ADC1	
	1	start_Conv. ADC2	
	2	start_out all DACs	
20400020h		status bit of ADCs.	During conversion bits are set to 1.
	0	end_of_conv ADC1	
	1	end_of_conv ADC2	
20400030h	0-11	data register ADC1	After end-of-conversion, result in last 12 bits.
20400040h	0-11	data register ADC2	
20400050h	0-11	data register DAC1	Values to converted should be written into last 12 bits. To start conversion set bit 2 at address 20400010h to 0.
20400060h	0-11	data register DAC2	
20400070h	0-11	data register DAC3	
20400080h	0-11	data register DAC4	
20400090h	0-11	data register DAC5	
204000A0h	0-11	data register DAC6	
204000B0h	0-15	digital input register	
204000C0h	0-15	digital output register	

6 I/O-register of the linkadapter in the PC

As mentioned in chapter 3.3 it is possible to set the base address with a DIP-switch. Based on this base address the linkadapter uses 7 I/O-addresses.

Address	**Function**
base address	data register FROM_LINK
base address + 1	data register TO_LINK
base address + 2	status register FROM_LINK
base address + 3	status register TO_LINK
base address + 16	bit 0 = reset
base address + 17	bit 0 = analyze
base address + 18	bit 0 = error message

7 Specifications

General Features:

Dimensions:	PC expansion board with 300 mm (11.81 inch) length, needs an 8 or 16-bit plug-in slot
Connections:	• 37-pin D-sub socket (female)at the rear of the board • optional: 37-pin D-sub add-on connector (male)
Power supply:	+ 5 V / 700 mA max.
Operating temperature range:	0...70 °C
Storage temperature:	-20...+70 °C
Relative humidity:	0...90% not cond.
Weight:	210 g

Analog Inputs:

Channels:	2 x 8 inputs
AD converter:	2 x ADS774 with integr. S&H
Conversion time:	8.5 µs
Resolution:	12 bits
Accuracy:	± 1 LSB
Max. sampling rate:	2 inputs with 100 kHz
Measurement ranges:	0...10 V, ±5 V, ±10 V (jumper-selectable)
Amplifiers:	1, 2, 4, 8 (programmable)
Input resistance:	100 kΩ
Offset error:	adjustable
Offset drift:	± 30 ppm/ C

Analog Outputs:

Channels:	2 to 6 max.
Resolution:	12 bits
Output voltage range:	0...10 V, ±5V, ±10V (jumper-selectable)
Output voltage:	5 mA per channel max.
Differential nonlinearity:	± 1 LSB
Relative accuracy:	± 1LSB
Offset error:	adjustable
Offset drift:	± 10 µV /°C
Gain drift:	adjustable
Settling time:	10 µs for 0.1%

Digital I/Os:

Digital outputs:	16 TTL
Digital inputs:	16 TTL
Trigger input:	1 TTL

All digital inputs and outputs are generated in an FPGA. Therefore it is easily possible to use the boards for specific applications (such as installation of counters, various trigger requirements).

Processor modules:

T225 (*ADwin-2*):

Processor:	INMOS T225 Transputer
Clock rate:	20 MHz
Memory:	64 kB
Links:	4

T400 (*ADwin-4*):

Processor:	INMOS T400 Transputer
Clock rate:	20 MHz
Memory:	4 or 8 MB
Links:	2

T450 (*ADwin-5*):

Processor:	INMOS T450 Transputer
Clock rate:	40 MHz
Memory:	4, 16 or 32 MB
Links:	4

T805 (*ADwin-8*):

Processor:	INMOS T805 Transputer
Clock rate:	25 MHz
Memory:	4 or 8 MB
Links:	4
Misc:	FPU with 3.2 MFlops

ADSP 21062 (*ADwin-9*):

Processor:	Sharc ADSP 21062
Clock rate:	40 MHz
Memory:	4, 16, 32 or 64 MB
Links:	1
Misc:	FPU with 120 MFlops

8 Bibliography

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