ADwin-light

Hardware Manual

Version 1.6

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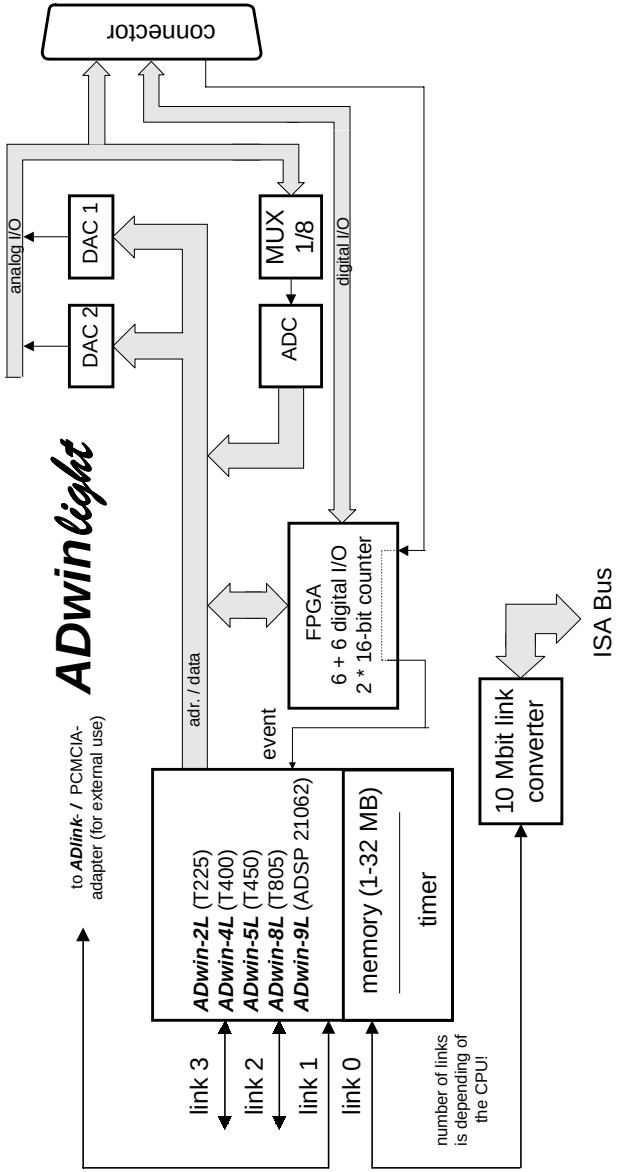

Picture 1: Block diagram of the ***ADwin-light*** board with changeable processor module

1 A Brief Overview

The ***ADwin-light*** board has a plug-in device for an 8/16-bit ISA-slot (Industry Standard Architecture) in an IBM-compatible PC. It needs a short slot.
The board includes its own processor for data acquisition and control and can be divided into two parts: the data acquisition board and the plug-in processor module.
As shown in the block diagram (Figure 1) the ADCs, DACs and the digital input/output registers can be directly accessed by memory addresses. Each CPU has one or more links for fast data transfer. Link 0 of each processor module is connected to the PC by a linkadapter component, which adapts the serial link connection to the 8-bit wide PC I/O bus. This link connection is also used for downloading the transputer program to the board memory.
The board has an ADC with 12-bit resolution and a conversion time of 8.5 µs. The ADC is connected to a differential amplifier and to a multiplexer with 8 input channels. The board includes two DACs with a 12-bit resolution. The DACs have a second buffer for latching so that with an instruction new data can be output on all DACs at the same time.
In addition the board contains 6 digital inputs and outputs, two 16-bit incremental counters and a trigger input.

2 Installation of the *ADwin-light* board

Please, pay attention to the following notes before installing the ***ADwin-light*** board:

- Touch the ***ADwin-light*** board only at the upper edge in order to avoid damage of the board components.
- The base address for the linkadapter on the ***ADwin-light*** board has the default address 150h. If you wish to set a different address, refer to chapter 3.3 (Setting the I/O-address).
- The input and output voltage ranges of the ADCs and DACs, respectively, have the default setting of ±10 V. If you wish to set a different voltage range, refer to chapter 3.1 (Setting the input voltage range of the ADC) or 3.2 (Setting the output voltage range of the DACs), respectively.

In order to install the ***ADwin-light*** board, follow the instructions below:

1. Make sure that the power switch on your PC is turned "off".
2. Open the computer chassis according to your PC manual.
3. Choose an empty plug-in slot and make sure that there will be enough space for installation of the ***ADwin-light*** board.
4. Remove the board access cover at the rear of the PC which belongs to the slot you have chosen to install the board.
5. Plug the ***ADwin-light*** board carefully in the slot chosen.
6. Secure the board access cover at the rear of the PC with the screws removed (under point 4).
7. Replace the computer chassis.

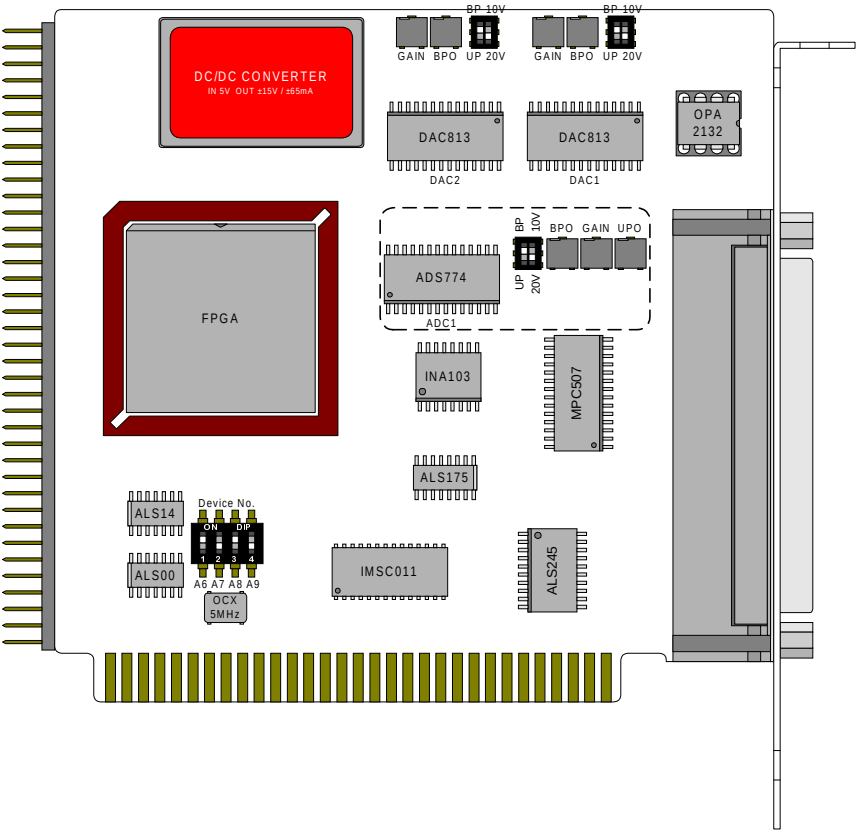

Figure 2: Location of jumpers and potentiometers to adjust the ADC

3 Jumper settings

3.1 Setting the input voltage range of the ADC

Each ***ADwin-light*** board has an ADC whose input voltage range can be adjusted by double SMD-switch (see Figure 2).
The following settings are possible:

BP / UP	10V / 20V	voltage range
BP	10 V	±5 V
BP	20 V	±10 V (default setting)
UP	10 V	0...10V
UP	20 V	not allowed

Example: Switch position for the input voltage range 0...10 V.

For calibration of offset and gain there are three potentiometers.

Note: These potentiometers were optimally adjusted after the final test of the board. For that reason we kindly ask you not to change the settings of the potentiometers unnecessarily, because this will lead to inaccuracy.

potentiometer	calibration of the...
GAIN	gain factor
BPO	offset (bipolar mode)
UPO	offset (unipolar mode)

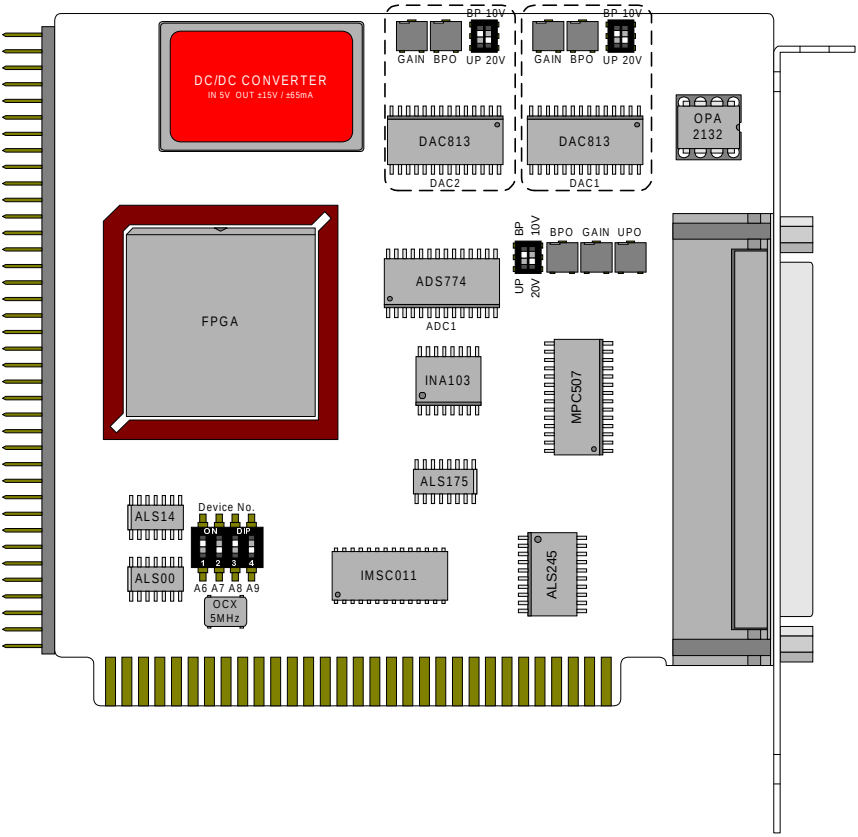

Figure 3: Location of jumpers and potentiometers to adjust the DACs

3.2 Setting the output voltage range of the DACs

Each ***ADwin-light*** board has two DACs whose output voltage range can be adjusted by the jumpers located just above the DACs (s. Figure 3).
The following settings are possible:

BP / UP	10V / 20V	voltage range
BP	10 V	±5 V
BP	20 V	±10 V (default setting)
UP	10 V	0...10 V
UP	20 V	not allowed

For calibration of offset and gain there are two potentiometers for each DAC.

Note: These potentiometers were optimally adjusted after the final test of the board. For that reason we kindly ask you not to change the settings of the potentiometers unnecessarily, because this will lead to inaccuracy.

potentiometer	calibration of ...
GAIN	gain factor
BPO	offset

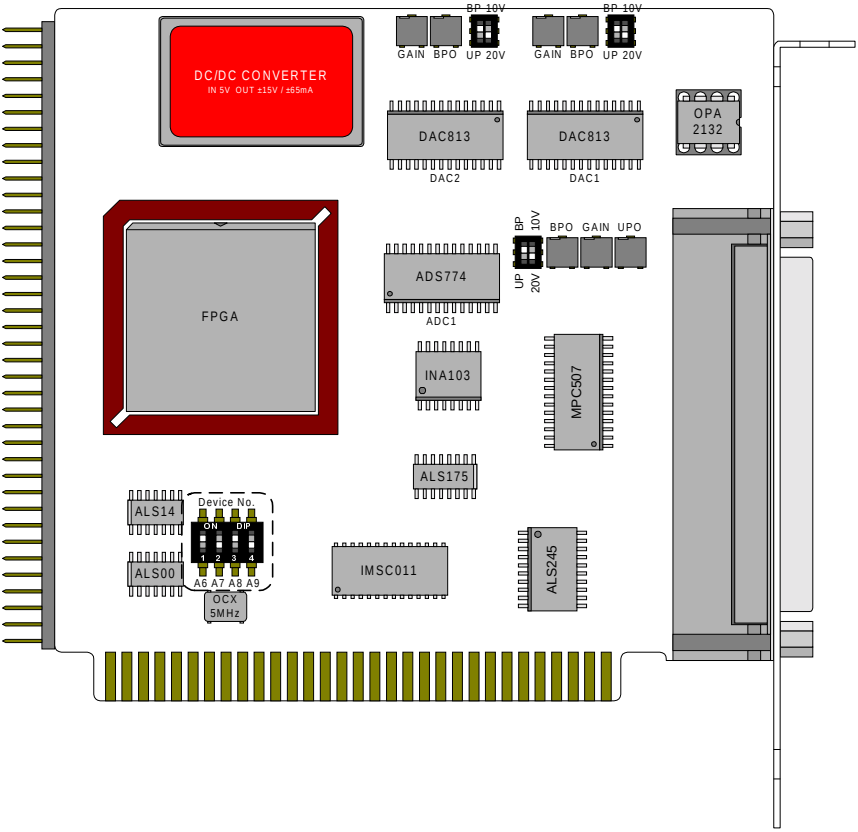

Figure 4: Location of the DIP switch to adjust the base address

3.3 Setting the I/O-address

Setting the I/O-address (base address for the linkadapter of the ***ADwin-light*** board) is made by the DIP switch called ADDR SWITCH (s. Figure 4).
The base address can be set on the DIP switches in binary code beginning with the sixth address bit. The fifth bit is always set to "high".

Example: The default setting 150h of the base address in ***ADbasic*** and on the ***ADwin-light*** board is in binary code 01 0101 0000b. The four least significant bits are always set to "low" and the fifth bit to "high". All numbers "1" of the four most significant bits are set in reverse order to "ON" on the DIP switches:

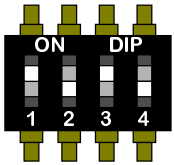

Figure 5: DIP switches with the base address 150h

base address	switch no.			
	1	2	3	4
150h	on	off	on	off
190h	off	on	on	off
210h	off	off	off	on
310h	off	off	on	on

Note: In case of using a different base address than 150h, this address has to be indicated in ***ADbasic*** and in the TestPoint objects.

3.4 Calculation of the ADC/DAC values

The ADC as well as the DACs used for the ***ADwin-light*** board have a resolution of 12 bits and divide the chosen measurement range into 4096 steps:

Adjust: 0...10 Volts
An ADC (DAC) value of 0 corresponds to the voltage of 0 Volts
An ADC (DAC) value of 4096 corresponds to the voltage of 10 Volts
An ADC (DAC) digit corresponds to 10 Volts/4096 = 2.44 mV

Adjust: ±5 Volts
An ADC (DAC) value of 0 corresponds to the voltage of -5 Volts.
An ADC (DAC) value of 2048 corresponds to the voltage of 0 Volts.
An ADC (DAC)value of 4096 corresponds to the voltage of +5 Volts.
An ADC (DAC) digit corresponds to10 Volts/4096 = 2.44 mV.

Adjust: ±10 Volts
An ADC (DAC) value of 0 corresponds to the voltage of -10 Volts.
An ADC (DAC) value of 2048 corresponds to the voltage of 0 Volts.
An ADC (DAC) value of 4096 corresponds to the voltage of +10 Volts.
An ADC (DAC) digit corresponds to 20 Volts/4096 = 4.88 mV.

The voltage can be calculated according to the following formula:

$$\text{Voltage} = \left(\text{Digits} - 2048_{\text{bipolarity}}\right) * \frac{\text{Voltage range}}{4096}$$

In case of using the unipolar setting the offset of 2048 digits has to be ignored.

4 Pin assignment

4.1 The I/O socket at the rear of the board

At the rear of the ***ADwin-light*** board there is a 37-pin D-sub socket. The socket has

- 2 analog outputs
- 8 analog inputs
- 6 digital inputs / 6 digital outputs
- 1 trigger input and
- the power supply (s. Figure 6)

On demand you can attach filter modules or isolation amplifiers to the connector.

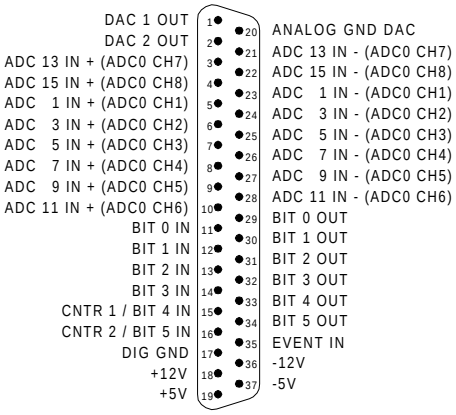

Figure 6: Pin assignment of the 37-pin D-sub socket

! **Attention**: The analog inputs are differential inputs. Make sure that the correct analog ground is used !

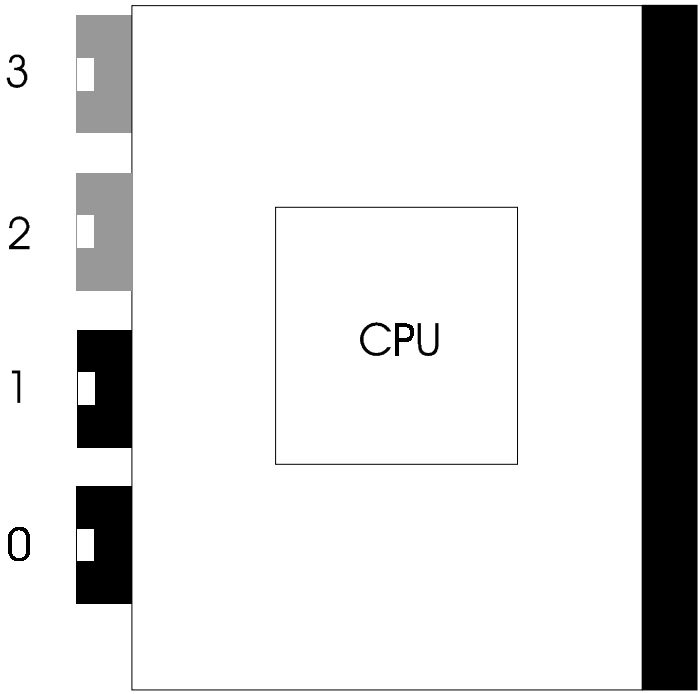

Figure 7 Location of the link connectors

4.2 The link connectors on the processor modules

The link connectors of the CPU are connected with the connectors at the front of the processor module. The assignment of the connectors to the links can be seen in Figure 7. Figure 8 shows the pin assignment of the link connector.
The ***ADwin-2L*** (T225), ***ADwin-5L*** (T450) and ***ADwin-8L*** (T805) have four links. The ***ADwin-4L*** board (T400) has two and the ***ADwin-9L*** (ADSP 21062) has one link.

Note: Link 2 at the ***ADwin-9L*** board is only used for stability when the board is installed in an ***ADwin-Pro*** System. With this link no data transfer is possible.

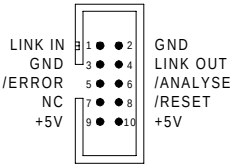

Figure 8: Pin assignment of the link connector

5 The I/O addresses on the CPUs

5.1 *ADwin-2L* (T225)

In order to get very short access times, the data and control registers of the ADCs and DACs are located directly in the memory address area of the CPU.

Address	Bit no.	Function	
7F00h	0-2	multiplexer control.	
7F08h	0 2	start conversion of ADC & DACs output. start_conv. ADC start_out all DACs	Write 0 in corresponding bit to start conversion. All three functions can be initiated with a single instruction simultaneously.
7F10h	0	status bit of ADC. end_of_conv ADC	During conversion bit is set to 1.
7F18h	0-11	data register ADC	After end-of-conversion, result in last 12 bits.
7F28h	0-11	data register DAC1	Values to converted should be written into last 12 bits. To start conversion set bit 2 at address 7F08h to 0.
7F30h	0-11	data register DAC2	
7F58h	0-5	digital input register	
7F60h	0-5	digital output register	

5.2 *ADwin-4L*, *ADwin-5L* and *ADwin-8L* (T400, T450 and T805)

In order to get very short access times, the data and control registers of the ADCs and DACs are located directly in the memory address area of the CPU.

Address	Bit no.	Function	
00h	0-2	multiplexer control (ADC)	
10h	0 2	start conversion of the ADC & DACs output. start_conv. ADC start_out all DACs	Write 0 in corresponding bit to start conversion. All three functions can be initiated with a single instruction simultaneously.
20h	0	status bit of ADC. end_of_conv ADC	During conversion bit is set to 1.
30h	0-11	data register ADC	After end-of-conversion, result in last 12 bits.
50h	0-11	data register DAC1	Values to converted should be written into last 12 bits. To start conversion set bit 2 at address 10h to 0.
60h	0-11	data register DAC2	
B0h	0-5	digital input register	
C0h	0-5	digital output register	

5.3 *ADwin-9L* (ADSP 21062)

In order to get very short access times, the data and control registers of the ADCs and DACs are located directly in the memory address area of the CPU.

Address	Bit no.	Function	
20400000h	0-2	multiplexer control (ADC)	
20400010h	0 2	start conversion of ADC & DACs output. start_conv. ADC start_out all DACs	Write 0 in corresponding bit to start conversion. All three functions can be initiated with a single instruction simultaneously.
20400020h	0	status bit of ADC. end_of_conv ADC	During conversion bit is set to 1.
20400030h	0-11	data register ADC	After end-of-conversion, result in last 12 bits.
20400050h	0-11	data register DAC1	Values to converted should be written into last 12 bits. To start conversion set bit 2 at address 20400010h to 0.
20400060h	0-11	data register DAC2	
204000B0h	0-5	digital input register	
204000C0h	0-5	digital output register	

6 I/O register of the linkadapter in the PC

As mentioned in chapter 3.3 it is possible to set the base address with a DIP switch. Based on this base address the linkadapter uses 7 I/O-addresses.

Address	**Function**
base address	data register FROM_LINK
base address + 1	data register TO_LINK
base address + 2	status register FROM_LINK
base address + 3	status register TO_LINK
base address + 16	bit 0 = reset
base address + 17	bit 0 = analyze
base address + 18	bit 0 = error message

7 Specifications

General Features:

Dimensions:	PC expansion board with 195 mm length, needs an 8 or 16-bit plug-in slot.
Connections:	37-pin D-type socket at the rear of the board
Power supply:	+ 5V / 700 mA max.
Operating temperature range:	0...70°C
Relative humidity:	0...90% not cond.
Weight:	150 g

Analog Inputs

Channels:	8 differential inputs
AD converter:	ADS774 with integr. S&H
Conversion time:	8.5 µs
Resolution:	12 bit
Accuracy:	± 1 LSB
max. sampling rates:	inputs with 100 kHz
Measurement ranges:	0...10 V, ± 5 V, ± 10 V selected by jumpers
Input resistance:	100 kΩ
Offset voltage:	adjustable
Offset-drift:	± 30 ppm/°C

Analog outputs:

Channels:	2
Resolution:	12 bit
Output voltage range:	0,... 10 V, ±5 V, ±10 V selected by jumpers
Output voltage:	max. 5 mA per channel
Relative accuracy	± 1 LSB
Differential nonlinearity	± 1 LSB
Offset	adjustable
Offset drift	10 µV/°C
Settling time	10 µs for 0.1%
Gain drift	adjustable

Digital I/Os:

Digital outputs	6 TTL
Digital inputs	6 TTL
Trigger input	1 TTL
16-bit counter	2 TTL
Output current	max. 10 mA per output
pull-down resistors	10 kΩ (pull-up)

All digital inputs and outputs as well as the two counters and the trigger logic are generated in a FPGA.

Processor modules:

T225 (*ADwin-2L*):

Processor:	INMOS T225 transputer
Clock rate:	20 MHz
Memory:	64 KB RAM
Links:	4

T400 (*ADwin-4L*):

Processor:	INMOS T400 transputer
Clock rate:	20 MHz
Memory:	1, 4 or 8 MB RAM
Links:	2

T450 (*ADwin-5L*):

Processor:	INMOS T450 transputer
Clock rate:	40 MHz
Memory:	4, 16 or 32 MB RAM
Links:	4

T805 (*ADwin-8L*):

Processor:	INMOS T805 transputer
Clock rate:	20 MHz
Memory:	1, 4 or 8 MB RAM
Links:	4
Misc.	FPU with 3,2 MFlops

ADSP 21062 (*ADwin-9L*):

Processor:	Sharc ADSP 21062
Clock rate:	40 MHz
Memory:	4,16, 32 MB RAM
Links:	1
Misc.	FPU with 120 MFlops

8 Bibliography

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(very good and detailed description of the transputer
hardware, also recommendable for C-programmers!)