

ADwin-CO1

Counter expansion for *ADwin*-boards

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ADwin-CO1 counter expansion for ADwin Systems

Pin and address assignments

DAC 1 Output	1 •	
DAC 2 Output	2 • • 20	
DAC 3 Output	3 • • 21	
DAC 4 Output	4 • • 22	
Analog In 1 (ADC0 K1)	5 • • 23	
Analog In 3 (ADC0 K2)	6 • • 24	
Analog In 5 (ADC0 K3)	7 • • 25	
Analog In 2 (ADC1 K1)	8 • • 26	
Analog In 4 (ADC1 K2)	9 • • 27	
Analog In 6 (ADC1 K3)	10 • • 28	
Digital Input Bit 0	11 • • 29	Digital Output Bit 0
Digital Input Bit 1	12 • • 30	Digital Output Bit 1
Digital Input Bit 2	13 • • 31	Digital Output Bit 2
Digital Input Bit 3	14 • • 32	Digital Output Bit 3
Counter Input A	15 • • 33	Counter Input B
Counter Reset	16 • • 34	NC
Digital Ground	17 • • 35	Event
+12V	18 • • 36	- 12V
+5V	19 • • 37	- 5V

The 37-pin-D-socket at the rear of the card is equipped with the inputs for the up- and down counters instead of the digital inputs/outputs 4 and 5.

The TTL-inputs "Counter Input A" and "Counter Input B" are connected with the two quadrature encoders whose signals are shifted by 90 degrees.

A high pulse at the counter reset input clears the counter.

The **ADwin**-card includes a 16-bit up/down counter. In order to control the counter 3 I/O-addresses are necessary. The Enable-register is set on address 0E0h. If writing 1 into the register the counter will be cleared. 2 starts the counter and 0 stops it. The Latch-register is on address 0F0h. If writing 1 into this register the present count rate is latched. The counter does not stop counting during this process. The latch is read out on address 0D0h.

```
Rem Sample program for reading out the 16-bit V/R-counter
dim CO_ENABL, CO_LATCH, CO_REG as integer
dim co as integer
```

```
init:
```

```
CO_ENABL = 0E0H
```

```
CO_LATCH = 0F0H
```

```
CO_REG = 0D0H
```

```
poke CO_ENABL, 1 ' clear counter
```

```
poke CO_ENABL, 2 ' start counter
```

```
event:
```

```
poke CO_LATCH,1 ' latch count rate
```

```
co = peek(CO_REG) ' read out latch and write into PAR-1
```

```
par_1 = co
```